A *Ka*-Band GaAs Monolithic Phase Shifter

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Abstract—**The design and performance of a GaAs monolithic 180° one-bit switched line phase shifter test circuit for *Ka*-band operation is presented. A self-aligned gate (SAG) fabrication technique is also described that reduces resistive parasitics in the switching FET's. Over the 27.5–30 GHz band, typical measured differential insertion phase is within 10–20° of the ideal time delay characteristic. Over the same band, the insertion loss for the SAG phase shifter is about 2.5–3 dB per bit. The SAG fabrication technique holds promise in reducing phase shifter insertion loss to about 1.5 dB/bit for 30-GHz operation.**

I. Introduction

As GAAS MONOLITHIC technology progresses to higher frequencies, it becomes natural to consider the development of specific integrated-circuit functions which are required by potential millimeter-wave system applications. The applications that take greatest advantage of monolithic circuit implementation include phased array systems for communications and radar, where a large number of small low-cost circuits are needed. For such systems, an essential circuit function is phase shifting at the carrier frequency. This paper presents design considerations and experimental results for a one-bit 180° phase shifter test circuit in *Ka*-band. Specifically, the work is aimed at potential application in a phased array satellite receiver operating in the 27.5–30-GHz band. Because of the receiver application, consideration is made for small-signal operation only. The monolithic GaAs chip incorporates passive switching FET's and microstrip transmission lines. The use of passive FET's is vital for low dc power consumption.

The FET's are fabricated by direct ion implantation into undoped LEC material, while the microstrip transmission lines are formed on the semi-insulating substrate. Two fabrication approaches are discussed: a conventional power FET approach and a self-aligned gate technique which reduces resistive parasitics in the switching FET's. The latter is especially important for millimeter-wave circuits.

II. Design Considerations

A. Chip Description

The design of the 180°-bit test circuit is based on a switched transmission-line type of configuration using switching FET's to RF switch between two microstrip lines. The differential electrical length of these lines is equal to 180° at center band, i.e., phase shifting is accomplished by true time delay. The FET's are passive in the sense that no dc bias is applied to the drain and only a switching voltage (0, −6 V) is used at the gate [1]–[3]. For broad bandwidth and low sensitivity to variations in device parameters, the circuit utilizes a pair of SPDT switches realized by four, 300-μm gate-width FET's in shunt across the 50-Ω transmission lines with each FET located at a distance of $\lambda g/4$ (0.8 mm at 30 GHz on GaAs) from either the input or output T-junction.

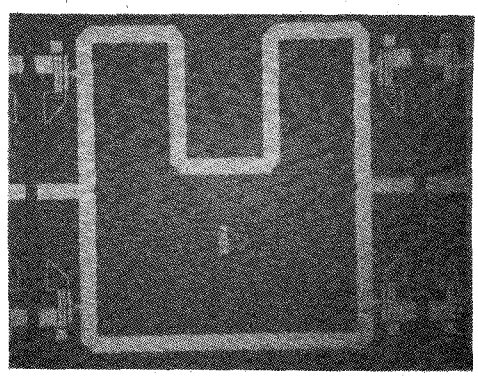

Fig. 1. Switched line phase shifter chip.

The circuit layout, shown in Fig. 1, is conservative in that the area required (chip dimensions are $3 \times 2.67 \times 0.2$ mm^3) has not been minimized. This was done to ensure that the coupling between adjacent sections of transmission lines would be negligible thereby facilitating evaluation of initial RF performance results. The 0.2-mm substrate thickness was chosen as a compromise between increased microstrip transmission-line loss and extraneous capacitive parasitics (thinner substrate), and increased circuit layout dimensions (thicker substrate). Since the circuit is passive, heat sinking of active elements is not an issue, and a relatively thick substrate can be used. As shown in Fig. 1, pads are provided at the edge of the chip for grounding. For these tests, ground connection is accomplished by a series resonant circuit consisting of an external 0.1-pF capacitor (bottom plate soldered to ground) and a mesh wire inductor connecting from the capacitor top plate to the grounding pad on the chip. To increase the high-impedance state ($V_g \cong -6$ V), a short section of line printed on the chip is used to resonate the pinchoff capacitance between drain and source ($C \cong 0.07$ pF) for each FET. High impedance to the gate terminal is provided by bonding wire inductance.

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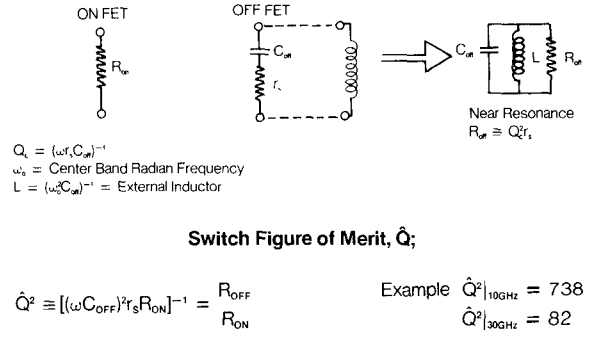


Fig. 2. Ideal equivalent circuits for ON and OFF FET's.

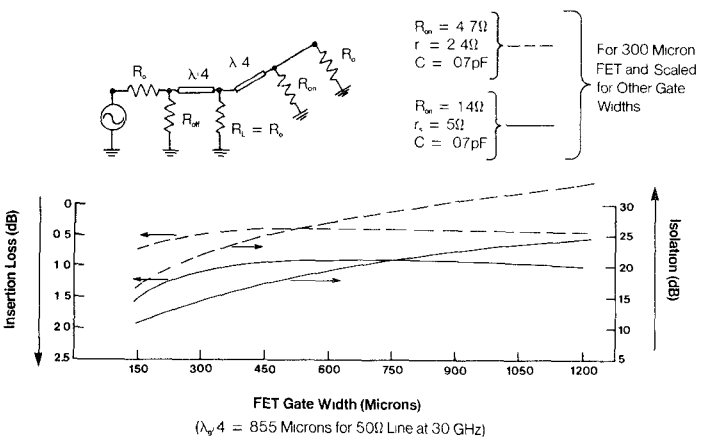


Fig. 3. Insertion loss and isolation in a SPDT switch as a function of FET gate width.

B. RF Losses

An important design consideration is the dissipative loss associated with the switches and the microstrip lines. As shown in the following, the dominant losses occur in the passive FET's.

Microstrip-line loss is calculated to be about 0.15 dB per wavelength at 30 GHz based on metal losses only and a gold thickness of 1.5 μm for a 50-Ω line on 0.2-mm-thick semi-insulating GaAs [4]. Experimentally, RF line losses measured at 30 GHz on GaAs ($\epsilon_r = 13$) and on sapphire ($\epsilon_r \approx 11$) substrates of the same thickness indicate comparable performance.

For the switching FET's, however, RF losses are much greater and are primarily associated with the parasitic resistances of the device. Fig. 2 shows simplified equivalent circuits for an ON and OFF FET, namely a single resistor for the ON (low-impedance) state and a series resistor capacitor combination for the OFF (high-impedance) state [2], [5]. The capacitor C_{off} is the total pinchoff capacitance between source and drain, and the resistor r_s is the total series residual resistance at pinchoff (undepleted channel resistance plus source and drain contact resistance). To increase the RF impedance of the OFF state, an inductor L parallel-resonates the RC combination. For this case, the effective RF OFF resistance at resonance R_{off} is closely approximated by $R_{\text{off}} = Q_c^2 r_s = (\omega r_s C)^{-2} r_s = (\omega C)^{-2} r_s^{-1}$. Note that the ratio $R_{\text{off}}/R_{\text{on}}$ is to first order, just the figure of merit as defined by Kurokawa and Schlosser for a switching device switching between two impedance states Z_1 and Z_2 [6]. For this case, $Z_1 = R_{\text{on}}$ and $Z_2 = r_s - j(\omega C)^{-1}$. Their figure of merit, denoted by $\hat{Q}$, is given by

$$\hat{Q}^2 = \frac{|Z_1 - Z_2|^2}{r_1 r_2} = \frac{(R_{\text{on}} - r_s)^2 + (\omega C)^{-2}}{R_{\text{on}} r_s}.$$

$\hat{Q}$ is a property of the device only and is invariant to any lossless impedance transforming imbedding circuit. If $(R_{\text{on}} - r_s) \ll (\omega C)^{-1}$ (which is a good approximation for switching FET's), then $\hat{Q}$ becomes

$$\hat{Q}^2 \cong (R_{\text{on}} r_s)^{-1} (\omega C)^{-2} = R_{\text{off}}/R_{\text{on}}.$$

From either point of view, i.e., $\hat{Q}$ or R_{off}, it is clear that for the same switching device both quantities degrade as the square of the frequency and have smaller values at millimeter-wave frequencies than they do at lower microwave bands. To maintain the figure of merit high it is essential to reduce R_{on} and r_s (and C if possible).

A specific example of an ideal RF switch incorporating conventional power FET's for the switching devices can illustrate the losses incurred at 30 GHz. For a typical 300-μm power FET, $R_{on} = 11$–14 Ω and with $C = 0.07$ pF and $r_s = 5$ Ω, R_{off} is about 1000 Ω at 30 GHz. By choosing these ON and OFF resistance values and using them in an ideal SPDT switch configuration as shown in the inset of Fig. 3, we can calculate the ideal insertion loss and isolation of a single switch at center frequency. Furthermore, by scaling R_{on}, r_s, and C for other gate widths, an estimate can be made of the best compromise between isolation and insertion loss. The scaling is straightforward, i.e., if the gate width is doubled, then R_{on} and r_s are halved, and C is doubled. Note that this leaves the figure of merit $\hat{Q}$ invariant. These considerations are summarized in Fig. 3, where the insertion loss and isolation at 30 GHz are calculated as a function of gate width for two different $\hat{Q}$ values. The curves are similar to those presented by Atwater and Sudbury [5], except that the constant $\hat{Q}$ curves are given specifically as functions of gate width. The impedance relation between the device impedance (gate width) and the normalizing impedance R_0 (the 50-Ω transmission lines) is analogous to the lossless imbedding network discussed by Kurokawa and Schlosser, i.e., for the same device $\hat{Q}$ different gate widths yield different values for insertion loss and isolation. Note that for the dashed curves which represent a reduction in R_{on} and r_s (14 Ω to 4.7 Ω and 5 Ω to 2.4 Ω, respectively), the loss is reduced by 0.6 dB at a gate width of 300 μm, for a single SPDT switch. For a four-bit switched line phase shifter this amounts to nearly 5 dB less insertion loss. As shown in the next section, such reductions in the parasitic resistance are possible using the self-aligned fabrication process.

To see the effects of reducing these losses at other frequencies, Table I gives the insertion loss comparison for 40, 30, 20, and 10 GHz for the two sets of FET resistance values given in Fig. 3. The arbitrary value of 20 dB for the isolation characteristic is chosen for all cases, and the resulting smallest gate width and insertion loss calculated.

TABLE I
IDEAL LOSSES IN A SINGLE SPDT SWITCH WITH 20 dB ISOLATION USING MINIMUM GATE WIDTH FET's

	300 micron FET Parameters*				
f (GHz)	R_{on} (Ω)	r_s (Ω)	$\hat{Q}^2$	Ins. Loss** (dB)	Gate Width (microns)
40	14*	5*	46.2	1.22	650
	4.7**	2.4**	286	0.59	235
30	14	5	82.1	0.9	680
	4.7	2.4	509	0.52	240
20	14	5	185	0.66	700
	4.7	2.4	1146	0.48	240
10	14	5	738	0.5	710
	4.7	2.4	4583	0.45	240

$\hat{Q}^2 = [(\omega C)^2 r_s R_{on}]^{-1} \equiv R_{on}/R_{on}$ *C_{off} = .07 pF, **Isolation = 20 dB } All cases

* Typical parameters obtained from conventionally fabricated FETs.
** Projected parameters expected from FETs fabricated with an optimized SAG technique.

It is seen that the reduction in parasitic FET resistances has the most significance at millimeter-wave frequencies. Not only does the insertion loss go down, but the required gate width also decreases. This is very important for reducing reactive parasitics at high frequencies since it implies smaller layout dimensions, hence, less capacitance to ground from layout metallization. It also means that the FET layout can be made much smaller than a wavelength. At microwave frequencies, the advantage of such small gate widths is not as important. Nevertheless, the lower resistances permit even lower insertion loss than shown in Table I if larger gate widths are allowed.

One approach to reduce the FET resistances is to use a self-aligned gate fabrication technique as discussed next.

III. Device Fabrication

Two processes have been used for fabricating switches: one process uses a standard power FET implant; the second uses a self-aligned gate process. The power FET approach uses standard GaAs FET processing including silicon ion implantation for the channel region, mesa etching for device isolation, a Au/Ge/Ni ohmic contact, and a recess etch for the gate. A Ti/Au overlay is used for the microstrip circuit and pad metal. FET's fabricated by this approach have a dc ON resistance of 11–14 Ω. FET's fabricated using the self-aligned gate process can give dc ON resistance as low as 4–6 Ω.

The self-aligned gate process is an approach that has been primarily used for digital IC's [7]. This process offers the advantage of lower ON resistance than the power FET switch. The self-aligned gate allows a low sheet resistance n^+ implant to be brought up very close to the gate, thereby minimizing the resistance of material in the gate–source and gate–drain regions. The refractory metal gate is made of Ti/W silicide which can withstand the subsequent high-temperature implant anneal. The first implant anneal is done at 850°C after the channel implant for good activation, the second anneal is done at 800°C after the n^+ implant. The lower temperature for the second anneal allows reasonable n^+ activation while minimizing degradation of the Schottky contact. Ohmic level metal is applied and sintered after the second implant anneal.

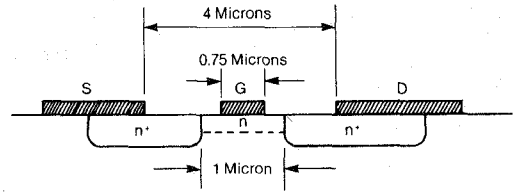


Fig. 4. Diagram of self-aligned gate switch FET showing parameters for resistance calculation.

The gate level metal is defined by an etch technique. Undercutting during the gate metal etch leaves a resist overhang which serves as an implant mask and separates the n^+ region from the gate. This technique gives self-aligned gate switches with reasonable gate breakdown voltages.

The ON resistance of the FET's is determined by three factors: the ohmic contact resistance, the sheet resistance of the n^+ implant, and the sheet resistance of the n or channel implant. For purposes of calculation, the dimensions shown in Fig. 4 are used. The source–drain ohmic contacts are separated by 4 μm and the n^+ implants are separated by 1 μm. The gate length is less than the separation between n^+ implants because a resist overhang is left beyond the gate edge after the gate is formed by reactive ion etching.

A typical measured value for the line resistance of the ohmic contacts is 0.063 Ω·mm, so a 300-μm gate width FET has a total contact resistance R_c of 0.42 Ω for the source and drain contacts. Typical values for the sheet resistance of the n and n^+ material are 660 Ω per square and 200 Ω per square, respectively. The total series resistance is 4.6 Ω for the self-aligned structure. By way of comparison, a conventional power FET would have the n material beneath the Schottky continued over the full 4-μm source–drain spacing so the total series resistance of the power FET switch would be 9.2 Ω, or twice the series resistance of the self-aligned gate FET.

Ultimately, the ON resistance of the self-aligned FET is limited by three factors. The first factor is the sheet resistance of the n^+ material. The resistance is limited by implant activation at high doses and by lateral diffusion of the implant species. The n^+ implant level will also affect the gate–source breakdown voltage of the switch. The second factor is the gate breakdown voltage. The resistance of the n layer beneath and immediately adjacent to the gate can be reduced by increasing the doping density thickness product of the channel. On the other hand, the doping density thickness product of the channel must be low enough so the device can be pinched off before gate breakdown occurs. The third factor is the contact resistance. A contact resistance corresponding to a line resistance of 0.05 to 0.1 Ω·mm is presently the best that is achieved. For most applications, the contribution of contact resistance to total resistance is small so there is little incentive to reduce contact resistance further.

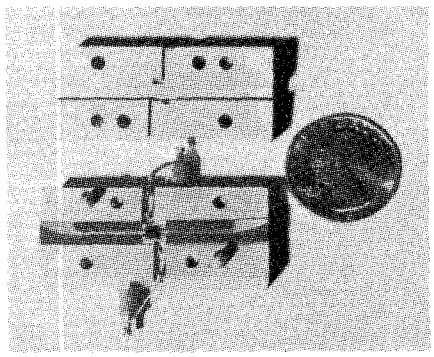


Fig. 5. Test fixture.

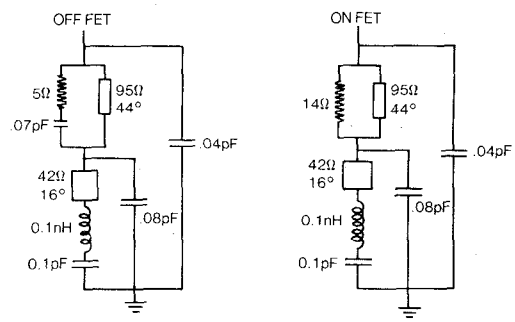


Fig. 6. FET switch circuit models including parasitics.

The TiW silicide gate metallization has a higher resistivity than the metals normally used for low-noise and power FET's. However, the gate resistance is not as critical for the present application since no RF signal is applied to the gate. The sheet resistance of the metal silicide is 6 Ω per square for a 4000-Å thickness. The metal resistivity is over an order of magnitude higher than gold or aluminum so it would not be suitable for low-noise FET's unless the unit gate width were made extremely small.

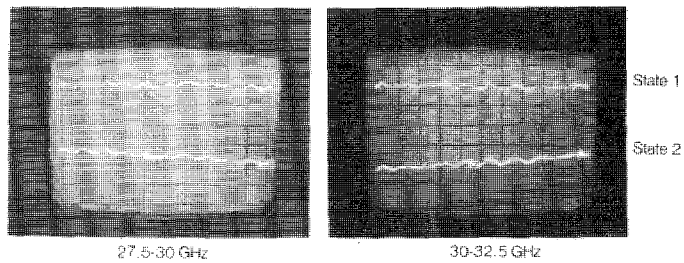


Fig. 7. Differential phase shift versus frequency for 180°-bit. Horizontal: 250 MHz/div, Vertical: 45°/div.

IV. Experimental Results and Comparison with Computer Calculations

A. Test Fixture

To interface the phase shifter chip with standard *Ka*-band circuitry, a test fixture having WR-28 waveguide input and output ports is used. Antipodal finline transitions fabricated on 0.25 mm thick RT/duroid are employed to transition from waveguide to microstrip [8], [9]. For a pair of back-to-back transitions including a 2.5-cm length of 50-Ω interconnecting transmission line etched on the same duroid card, the insertion loss is 0.6–0.8 dB from 26.5–37 GHz. For the phase shifter test circuit, the duroid card is cut in two, and each half soldered (at the ground plane side of the microstrip portion) to gold-plated brass blocks on the input and output side of the chip carrier block (see Fig. 5). To measure the insertion loss of this test fixture configuration, a 50-Ω microstrip line fabricated on a 0.13-mm-thick sapphire substrate is substituted for the phase shifter chip. In this way, transition losses from waveguide to microstrip on RT/duroid, as well as losses associated with the gold ribbon bond connection from the microstrip on duroid to the chip (mainly mismatch losses), can be taken into account. From 27 to 33 GHz, the measured test fixture loss is 1.4 dB. The test fixture with the phase shifter chip in place and the cover removed is shown in Fig. 5.

RF measurements of differential phase and insertion loss were performed on a network analyzer using the Hewlett-Packard 26–40-GHz waveguide reflection–transmission test set. A scalar reflectometer test set was also used to measure insertion loss and return loss.

B. Results with Conventionally Fabricated Phase Shifters

To compare the experimental results with the results of a computer analysis, a more elaborate circuit model that includes the ideal FET model discussed earlier, as well as additional circuit elements that represent our best estimate of the reactive and resistive circuit losses, is used. Fig. 6 shows the networks that are connected in shunt (four places) across the pair of 50-Ω transmission lines that constitute the switched lines of the 180°-bit phase shifter. In both networks, the section of 90-Ω line represents the printed loop that resonates the pinchoff capacitance during the OFF state. The 0.04 and 0.08-pF capacitors are part of the reactive parasitics associated with the layout metallization (assumed $Q_c = 100$), and the 0.1-pF capacitor is the external porcelain chip capacitor (assumed $Q_c = 50$) that series resonates the mesh wire inductance and provides an RF ground in close proximity to the "source" pad of each FET. Losses in the microstrip lines are also included in all the calculations.

Fig. 7 shows the measured differential phase shift for a conventionally fabricated phase shifter from 27.5 to 32.5 GHz. Over the frequency range of 27.5–31 GHz, the measured phase shift is within approximately 10–15° of the ideal time delay characteristic, i.e., a straight line through the origin with a slope of 6°/GHz corresponding to 180° at 30 GHz. (It should be noted that the 180° phase shifter test chip was originally designed for a center frequency of 30 GHz.) Beyond about 30 GHz, the measured differential phase changes slope and begins to decrease. Computer calculations of the phase shifter circuit using the FET models that include circuit parasitics have shown that such a decrease can result because of parasitic shunt capacitance loading the transmission line. Specifically, it was found that the metallization pattern of each FET contributes about 0.1–0.15 pF of shunt capacitance to ground, and when included in the calculations, a change of

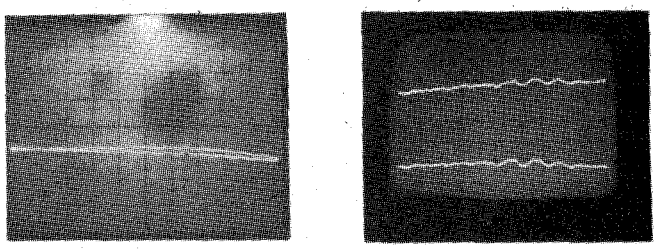
slope for the differential phase characteristic does indeed occur beyond 30 GHz. These results bring out the importance of minimizing the FET layout (by using smaller gate widths consistent with adequate isolation and insertion loss performance) and incorporating the FET into the transmission line as much as possible (via holes, if practical in a 0.2-mm-thick substrate, would help). Increasing the substrate thickness results in a larger layout and is therefore less desirable. Extraneous shunt capacitance also contributes to mismatch loss.

Calculated values of the phase shifter insertion loss (when transmission-line losses and the parasitic capacitances of the FET layout metallization are included) lie between 2.5 and 4.5 dB across the 27–32-GHz band using values of $R_{on} = 14\ \Omega$, $r_s = 5\ \Omega$, and $C = 0.07$ pF. Taking into account the 1.4-dB fixture loss, typical measured results lie between 3.2 and 5.5 dB across the same band. The 0.5–1-dB discrepancy may be due in part to not having all four of the FET's have exactly the same characteristics as is assumed in the computer calculations. The 14-Ω ON resistance was measured on the curve tracer for single FET's in the test pattern areas. The 5-Ω series residual resistance was based on dc measurements of source and drain contact resistances and an estimate of the resistance of the undepleted channel at pinchoff. The channel and parasitic resistances of individual FET's of the phase shifter may have different values. In addition, some substrate surface conduction was observed on some of the wafers on which phase shifter circuits were fabricated. Although mesa etching was used for isolation, increased loss due to surface conduction could still occur in the switching FET's. Such losses would be especially significant in the ON branch of the phase shifter when the shunt FET's are in their high-impedance state.

C. Results with Phase Shifters Fabricated by the Self-Aligned Gate (SAG) Technique

As discussed above, the self-aligned gate technology is one approach to reducing the resistive losses in switching FET's, especially at millimeter-wave frequencies. The experimental results reported in this section were obtained using the same 180° one-bit phase shifter test circuit of Fig. 1, but the chips were fabricated by means of the SAG technique.

The reduced parasitic resistances in SAG devices is clearly indicated by the dc FET characteristic of 300-μm gate width FET's taken from test pattern areas of the SAG phase shifter wafer. Instead of the usual 11–14-Ω ON resistance (slope of $V_g = 0$ drain characteristic) observed with conventional power FET's, a resistance of 7.8 Ω is obtained. Furthermore, I_{dss} is measured to be 225 mA instead of the usual 110–120 mA for 300-μm conventional power FET's. The improvement in RF results is shown in Fig. 8(a), where the phase shifter insertion loss, including test fixture losses, is measured from 27.5 to 32.5 GHz. Fig. 9 shows the comparison between the calculated and measured results including the 1.4-dB test fixture correction. As shown in the figure, the calculated values are based on



(a) (b)

Fig. 8. Insertion loss and phase shift characteristics for SAG fabricated phase shifter. (a) Insertion loss. Vertical: 5 dB/div, Reference: Center line, Horizontal: 500 MHz/div; 27.5–32.5 GHz. (b) Differential insertion phase. Vertical: 45°/div, Horizontal: 250 MHz/div; 27.5–30 GHz.

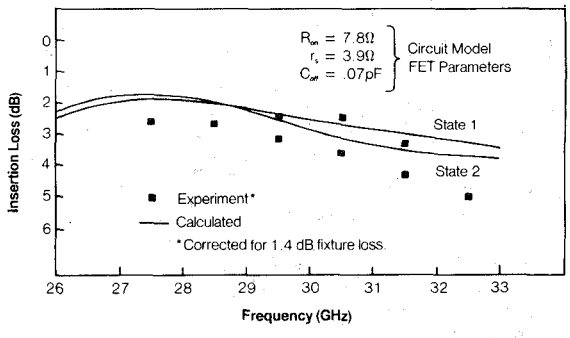


Fig. 9. Comparison of measured insertion loss results with computer calculations.

the values of the FET parameters measured off test FET's on the SAG wafer.

By comparison with the previous results, a reduction in insertion loss of about 1–1.5 dB across the entire band is achieved. The reasonable agreement between measured and calculated values justifies the use of our simple equivalent circuit model for the ON and OFF FET's.

Fig. 8(b) shows the measured differential insertion loss for the SAG phase shifter, from 27.5 to 30 GHz. Over this band, the phase is within 20° of the calculated curve. This discrepancy is greater than seen on previous runs. Although the exact cause of this discrepancy is not yet known, it is believed that it is not related to the intrinsic SAG process itself, but rather is indicative of the preliminary nature of these first results. With a better refined SAG process, it is expected that the insertion phase will track more accurately the theoretical values.

Finally, to estimate the insertion loss of a 1-bit phase shifter having FET's with characteristics comparable to the best expected SAG results, the computer calculations were repeated for $R_{on} = 4.7\ \Omega$, $r_s = 2.4\ \Omega$, and $C = 0.07$ pF, leaving all other elements (including capacitive parasitics) unchanged. The calculated results predict an insertion loss of 1.4–2.2 dB from 27–30 GHz. With a reduction in capacitive parasitics, an insertion loss of about 1.5 dB per bit across the same band should be possible.

V. Conclusions

By using a simple equivalent circuit for the ON and OFF FET's in a 180° switched-line phase shifter, an analysis is made to show how the FET parasitic resistances and gate

width are related to switch insertion loss and isolation performance at 30 GHz, as well as at other frequencies. The analysis shows that the loss is dominated by the resistive dissipation occurring in the channels of the switching FET's, which is especially high at millimeter-wave frequencies. At the higher frequencies, a reduction in the FET parasitic resistances R_{on} and r_s not only reduces the insertion loss but allows one to use smaller gate width FET's to achieve acceptable insertion loss and isolation performance. Since extraneous parasitic shunt capacitance associated with the details of the FET layout contribute significantly to the total insertion loss (primarily as mismatch loss), the possibility of employing FET's with smaller gate widths is an important design consideration.

An approach to reducing the intrinsic resistive losses in the FET is to make use of a self-aligned gate technology. By comparison with conventionally fabricated FET's, a reduction in the open channel resistance by about a factor of 1.5 to 2 has been demonstrated for a switching FET obtained from a test pattern area of a self-aligned run of phase shifter circuits. Similarly, the RF insertion loss results of conventional and SAG fabricated phase shifters were compared with each other, as well as with computer simulations of the phase shifter circuit. Generally, more than 1-dB improvement was observed for the SAG devices. The reasonable correlation with calculated values justifies the use of the circuit models. Using this model to predict the performance of phase shifters having optimized SAG parameters, it is expected that 30-GHz phase shifters could be fabricated to have insertion loss of about 1.5 dB/bit. Results obtained on the SAG phase shifters to date have achieved about 2.5 dB/bit over the 27.5–30-GHz band. Over this frequency range, the differential phase shift is within 10–20° of the ideal time delay characteristic for both types of phase shifters.

For system applications requiring high efficiency such as in satellite-borne communications receivers, the self-aligned gate fabrication technique is a promising technology for implementation in switching circuits at millimeter-wave frequencies.

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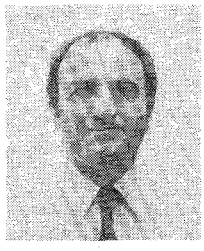
From 1963 to 1966, he worked as a Circuit Design Engineer at Raytheon Missle Division, Bedford, MA. From 1966 to 1971, he was a Lab Instructor and Teaching Assistant at Purdue. Since 1971, he has worked at Honeywell, Inc., Minneapolis, MN, in a variety of areas including plated wire memories, magnetic bubbles, fiber optics, and laser diodes. He is presently working on the development of *Ka*-band GaAs MESFET's and monolithic IC's.



A. Contolatis was born in Gravia, Greece, on April 23, 1937. He received the B.S. degree in electrical engineering from the University of Minnesota, Minneapolis, MN.

From 1956 to 1967, he served in the Greek Air Force working in telecommunication and radar systems. In 1969, he joined Honeywell Inc., and worked in the ferrite materials and fiber-optic programs. Since 1978, he has been engaged in the development of GaAs monolithic circuits.

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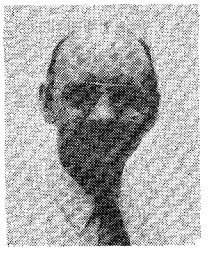

M.S. degree in electrical engineering, the M.S. degree in physics, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1969 and 1977, respectively.

From 1961 to 1966, he was a Communications Officer in the U.S. Air Force. At the University of Michigan, he was a Research Assistant in the Electron Physics Laboratory from 1970 to 1977. Since 1977, he has been with Honeywell, Inc., developing millimeter-wave devices.

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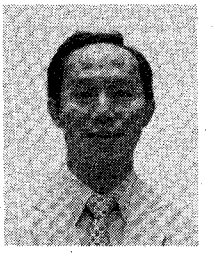

Ph.D. degree in electrical engineering from the University of Michigan, in 1974.

From 1969 to 1973, he was a Research Assistant at the Electron Physics Laboratory, Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, where he worked on research programs on nonlinear operating characteristics, bias modulation, and self-mixing properties of IMPATT diode oscillators. From 1974 to 1978, he was with the Torrance Research Center, Hughes Aircraft Company, where he worked on millimeter-wave low-noise scanning receivers, high-power pulsed IMPATT sources, and dielectric image-guide integrated circuits. He joined Honeywell Inc., in 1978. He is the Head of GaAs Analog Electronics Section in the Honeywell Corporate Technology Center. He is responsible for the development of microwave and millimeter-wave monolithic integrated circuit technology.

12-GHz-Band Low-Noise GaAs Monolithic Amplifiers

TADAHIKO SUGIURA, HITOSHI ITOH, TSUTOMU TSUJI, AND KAZUHIKO HONJO, MEMBER IEEE

Abstract — **One- and two-stage 12-GHz-band low-noise GaAs monolithic amplifiers have been developed for use in direct broadcasting satellite (DBS) receivers. The one-stage amplifier provides a less than 2.5-dB noise figure with more than 9.5-dB associated gain in the 11.7–12.7-GHz band. In the same frequency band, the two-stage amplifier has a less than 2.8-dB noise figure with more than 16-dB associated gain. A 0.5-μm gate closely spaced electrode FET with an ion-implanted active layer is employed in the amplifier in order to achieve a low-noise figure without reducing reproducibility. The chip size is 1 mm × 0.9 mm for the one-stage amplifier, and 1.5 mm × 0.9 mm for the two-stage amplifier.**

I. Introduction

RECENT ADVANCES in GaAs technology have made monolithic microwave integrated circuits (MMIC's) more practical. Promising applications for this technology include inexpensive receiver front ends for direct broadcasting satellite (DBS) systems [1], [2]. This paper describes design considerations, the fabrication process, and performances for newly developed one- and two-stage 12-GHz-band low-noise GaAs monolithic amplifiers for use in DBS receivers. For MMIC's used in DBS receivers, reproducibility improvement and chip size reduction are essential in order to achieve low cost. A low noise figure is also required for the amplifiers, because it determines the overall receiver noise figure. In this work, most efforts were focused on achieving these requirements.

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II. FET Design

The main reason for poor MMIC reproducibility is the variation in FET characteristics caused by nonuniformity of active layers. To improve uniformity, an ion-implantation technique was employed to form the active layers, although epitaxially grown active layers are believed to be better for low-noise FET's. In conventional MMIC's, a recessed gate structure has been widely used for reducing unfavorable source resistance [5]. The gate-recessing process, however, degrades uniformity of active layers. To overcome this difficulty, a closely spaced electrode (CSE) FET structure [3], [4] was introduced. In the CSE FET, source–gate and drain–gate spacings are shortened to 0.5

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